Embedded Software Engineering

Topic 4

Task-level Modeling of Embedded Applications

Task-level Modeling

- System models
- ♦ Task modelling in D(S)CS
- Task modelling in CoCS
- Task modelling in HCCS
- An overview on graphics notations and languages for CCS



- ❖ Diffeteentofnadelszesent the system from different perspectives dded Systems
 - External perspective showing the system's
- System reader ling in the locality of the system understand the functionality of the system and madels are fused to customers
 - customers

 Structural perspective showing the system or data architecture



Structured Methods

Structured methods incorporate system modelling as an inherent part of the method

Methods define a set of models, a process for deriving these models and rules and guidelines that should apply to the models

Model Types

- Destaspiroates in monte del Showing how the tidies in a peccesse drat differentes taties
- Strowing hav systities are acomposed whits. other entities
- Architectural model
 Showing principal sub-systems

Context Models

Context models are used to illustrate the boundaries of a system:

- Social and organisational concerns may affect the decision on where to position system boundaries
- Architectural models show a system and its relationship with other systems

Process-Oriented Models

- A process-oriented model is based on a set of interacting processes (tasks) running under a real-time kernel or a static schedule.
- Process-oriented models emphasize the functional decomposition of real-time systems.
- Process-oriented models address naturally the problems of scheduling and schedulability analysis.

Object-Oriented Models

Object-oriented specifications emphasize structural decomposition.

System is conceived as a composition of interacting objects.

Behavioural Models

- Behavioural models are used to describe the overall behaviour of a system.
- Two types of behavioural model are shown here:
 - Computational models showing how data and signal transformations are organized
 - Control-flow models that show the systems response to events and time passage

Both of these models are required for a description of the system's behaviour.

Component-Oriented Models

Components are represented in the context of control systems as:

- Schedulable computational element having well defined behaviour and having a set of interfaces to communicate to its environment
- A main difference form object-oriented model is that the component is self-dependent and maybe it is a set of objects

Types

- Symbolic execution of state machines –
 Programmable Logic Controller (PLC)
- State-logic execution –
 State Logic Controller (SLC)

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Automata Models

♦ Finite State Machines

♦ Petri Nets

Finite State Machines

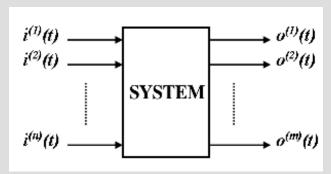
Automata Models

Finite State Machines

FSethereryappficatelestateproblemines (FrSeth) field of cesses archethowith models and ical models and it has been widely applied in whose significance estates. SM's theory is that its models are not confined to any particular scientific area.

Preliminary Definitions:

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Definition:

A Finite State Machine M is a 5-tuple

R(s, i, s', o) means that for input *i*, there is a transition from state s to state s' pthelinitial state at a lso denoted by
$$s \rightarrow M$$

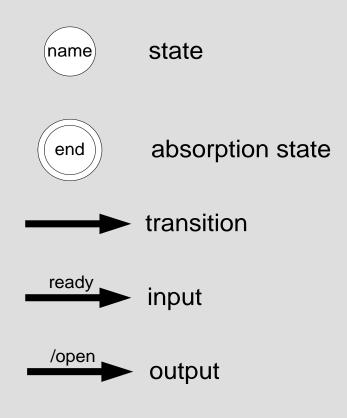


Definition:

A **Finite State Machine** (FSM) can be interpreted as an automaton over the alphabet $I \times O$.

The set of all pairs (I_k , O_k) such that sequence O_k is produced as output on applying sequence I_k as the input, gives the language of the automaton.

Graphical Notation:

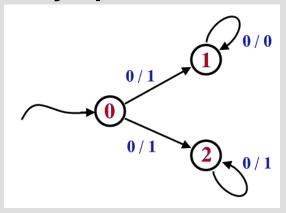


Classification

Pate Pate Pate (NPS (N)) (PNDFSM)

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Otherwise, it is said to be incompletely specified.



In the automaton sense

- Both DFSM and PNDFSM are deterministic
 The underlying automaton for a PNDFSM makes a unique transition for a given 1 / O pair.
- NDFSM is non-deterministic

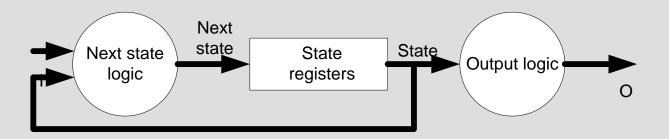
Time-discreetness

* Styndstation and the system tather system to the system to the confidence of the c

Types:

- ♦ Moore machine
- Mealy machines
- ♦ Medvedev machine

Moore machine



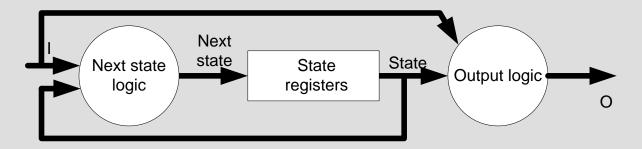
Moore machine is a 5-tuple:

$$M = (S; I; O; \delta; \lambda)$$

 $\lambda: S \to O$

Output function -> the output vector (O) is a function of state vector (S)

Mealy machine



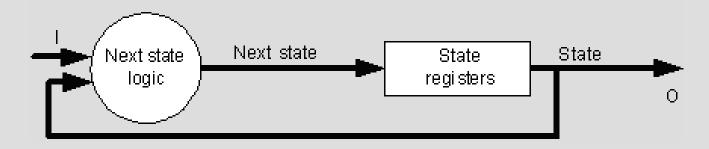
Mealy machine is a 5-tuple:

$$M = (S; I; O; \delta; \lambda)$$

$$\lambda: S \times I \rightarrow O$$

Output function -> the output vector (O) is a function of state vector (S) and the input vector (I)

Medvedev machine



Medvedev machine is a 5-tuple:

$$M = (S; I; O; \delta; \lambda)$$

 $\lambda : S = O$

Output function -> the output vector (O) resembles the state vector (S)

Modelling Aspects:

- Medvedev is inflexible
- Moore is preferred because of safe operation.
- Mealy is more flexible but has disadvantages -> possible spikes, long paths.

Every Moore automaton can be transferred to Mealy and vice versa.

Petri Nets

Automata Models

Petri Nets

Petrien Etectron in Steet to confidence to be as in path term at ical model.

- ♦ ban evaluation method (called the firing rule) for describing the *dynamic* behaviour of the system based on these relationships.

Definition 1:

The triple X = (P, T, F) is a set, where:

- A graphical notation:
- Fachielement of the set is connected to at least one
- for transitions rectangle $F \subseteq (P \times T) \cup (T \times P)$ for transitions - rectangle $F \neq \phi \cap (\forall x \in f)$ finite state of $f \in F$
- In the set X there are no pair of positions incident to one and the same transition:

$$\forall p_1, p_2 \in P : (p_1^* = p_2^*) \land (p_1^* = p_2^*) \Rightarrow (p_1 = p_2)$$

*x : the set of its input elements $\{y \mid yFx\}, \forall x \in X$

 x^* : the set of its output elements $\{y \mid xFy\}$, $\forall x \in X$



Definition 2:

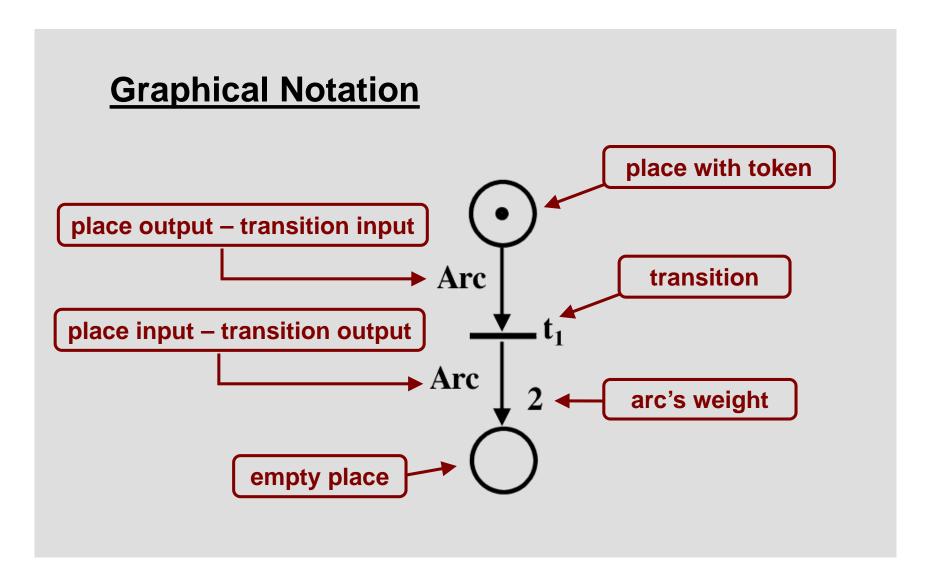
A Petri nets in a five-tuple $PN = (P, T, F, W, M_0)$:

 $M_0: P \rightarrow \{0, 1, 2, ...\}$ the initial marking

 $M_0(p)$, $p \in P$ is the marking (i.e. numbers of tokens) of the place p.

Notations:

- ♦ *t: the set of input places of transition t. That is the set of places p such that (p, t) ∈ F
- \diamond t*: the set of output places of transition t. That is p such that $(t, p) \in F$
- ⋄ *p : the set of input transition of place **p**. That is the set of transitions **t** such that (t, p) ∈ F
- \diamond p*: the set of output transition of place **p**. That is **t** such that $(p, t) \in F$



Activities:

⋄ The transition t ∈ T is enabled if for some marking M for PN,

$$\forall p \in {}^*t : M(p) \ge F(p,t)$$

that means whatever place **p** from the input places of some transition **t** contains number of tokens greater or equivalent than the weight of the arc connecting them.

Activities:

- Firing the transition t in the context of marking M results to new marking M' as follows
 - removing W(p,t) tokens from each, meaning that from each input place p of the transition t are removed number of tokens equal to the weight of the arc connecting the place and the transition;
 - adding W(p,t) tokens to each, meaning that to each output place p for the transition t are added number of tokens equal to the weight of the arc connecting the transition and the place.

Activities:

♦ Firing the transition t in the context of marking M results to new marking M' as follows:

$$\forall p \in P : M'(p) = M(p) - F(p,t) + F(t,p)$$

equivalent to

$$M' = M - {}^*F(t) + F^*(t).$$

Activities:

On the set of markings M is introduced relation \longrightarrow for direct marking sequence as:

$$M \longrightarrow M' \Leftrightarrow \exists t \in T : (M \ge^* F(t)) \land (M' = M - F(t) + F(t))$$

If M' follows directly form M as a result of firing the transition t it is said that

$$M \xrightarrow{t} M'$$

Activities:

Marking M' is reachable from M if there is a sequence of markings M, M_1 , M_2 , ..., M' and sequence of transition firings $\tau = \langle t_1 t_2 ... t_k \rangle$ on the T, so that

$$M \xrightarrow{t_1} M \xrightarrow{t_2} M \xrightarrow{t_3} \dots \longrightarrow M \xrightarrow{t_k} M'$$

We will say $\tau = \langle t_1 t_2 \dots t_k \rangle$ to be a vector of firings.

Activities:

To say that M' is reachable from M it is written

$$M \longrightarrow M'$$
 or $M \stackrel{\tau}{\longrightarrow} M'$

A set of markings $\{M' \mid M \rightarrow M'\}$ reachable in the set PN from the marking M is represent as R(PN,M).

The set $R(PN) = R(PN, M_0)$ or the set of all markings reachable from the initial marking M_0 is named

the reachable places set.

Incidence matrix:

The matrix $A = [a_{ij}]$ is a $n \times m$ matrix and for each a_{ii} is given

$$a_{ij}=a_{ij}^{+}-a_{ij}^{-}$$

where:

- $a_{ij}^{+} = w(i,j)$ It is equal to the weight of the output arc from transition j to its output place i.
- $a_{ij} = w(j,i)$ it is equal to the weight of the input arc from place i to its output transition j.

Incidence matrix:

The incidence matrix can be represented as two different matrixes A^+ and A^-

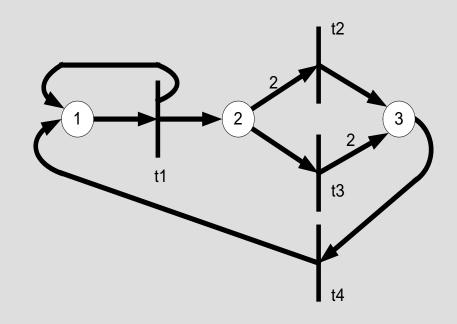
- → A⁺: represents the weight of output arcs from every transition to every place,
- → A⁻ : represents the weight of output arcs from every place to every transition.

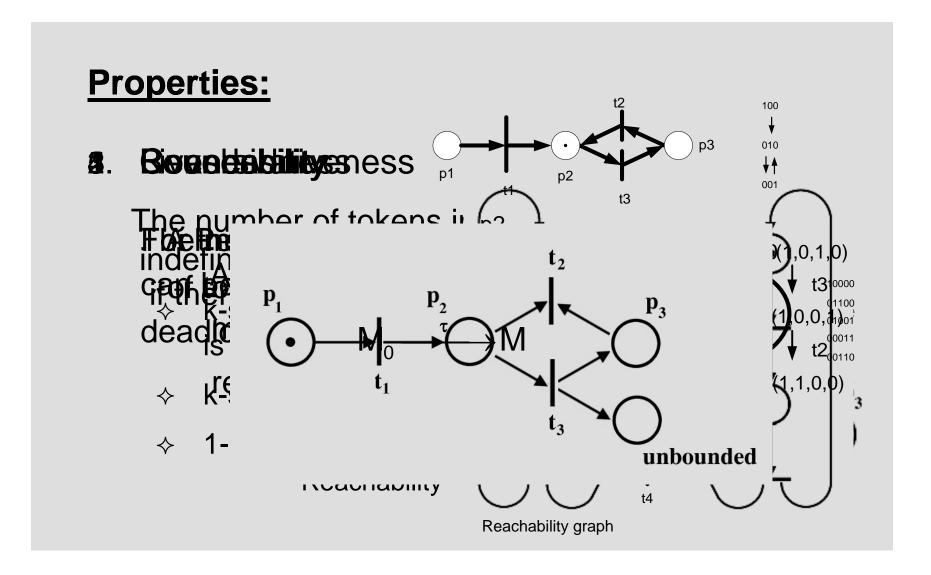
Incidence matrix: Example

A sample Petri net and corresponding matrixes of incidence:



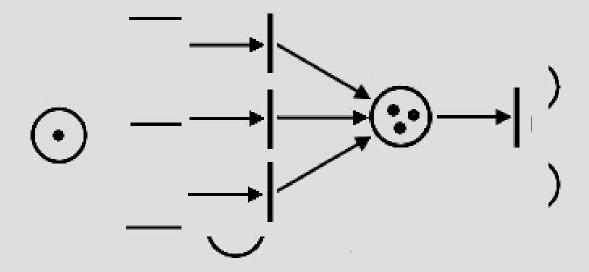
	Hp ¹¹	19 22	tgg.	3 t	1
P ₁₁	Cl	01	∞	C	
12/2	0	-2 2	111	C	
13 3	0	-00	022	1	
t _4	11	0	-10		





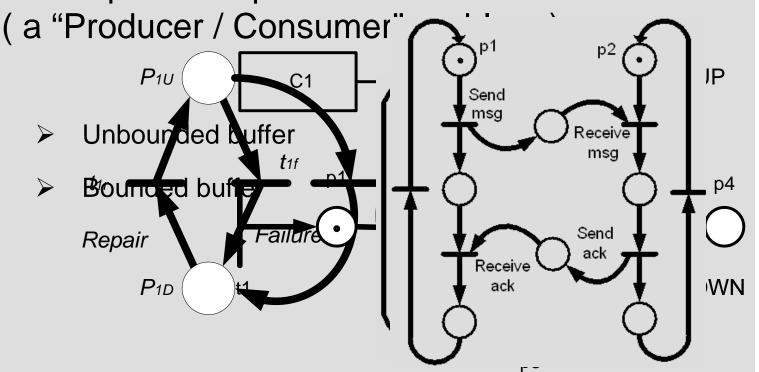
In progress modelling:

3. Standingtonibatidentetioninist



Examples:

3. Actors spriocaellis notion blooked Lincoited buffer



Analyzes:

- Structural analysis techniques
 - Incidence matrix
 - > T- and S- Invariants
- State Space Analysis techniques
 - Coverability Tree
 - Reachability Graph

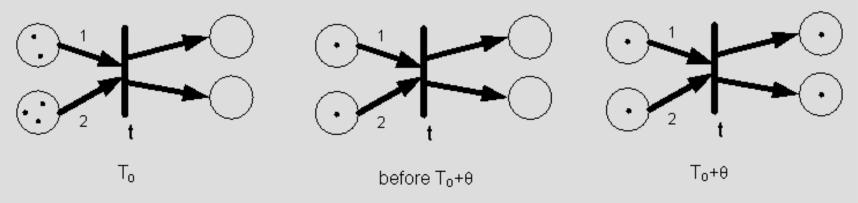


Advantages and Disadvantages:

- Eleoste himographic in precipation in the precipation of the precipation in the p
- concurrency, conflicts and mutual exclusion begy sleng, to state explosion situation thus making graphical and mathematical
- Ferresegantation enables easy understanding of structure of complex systems;
- Hard to follow changes in system structure.
 Analyzes possible for detecting deadlocks,
- Analyzes possible for detecting deadlocks, starvations, overflow, irreversive situations, etc;
- Performance analyzes based of deterministic timed Petri nets or stochastic timed Petri nets;

Timed Petri Nets

 \div Letingings of implemental time east one are as a result of a firing (p,t) tokens from every at time T_0 .



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Definition:

The programmable logic controller is a reconfigurable software architecture that has been specifically developed for synchronous (time-driven) sequential controllers.

Characteristics:

The PLC emulates the circuit diagram of the state machine (and *indirectly* – its behaviour).

Implemented by periodical computation of two sets of Boolean functions describing the logical structure of the state machine:

- state transition functions
- output functions (or state transition functions used in conjunction with control memory).

Characteristics:

Reconfiguration can be done in several ways:

- By special-purpose graphical languages, such as function block diagrams and ladder diagrams defined in standard *IEC 61131-3* in order to specify the structural model of the implemented controller, which is subsequently translated into executable code
- By generating a data structure containing the machine-level description of controller functions, which is interpreted subsequently by a standard software routine, i.e. the state machine driver.

Characteristics:

Binary decision diagram's are used for table description of controller's functions:

Binary decision diagram (BDD) is a special technique used to represent and efficiently compute Boolean functions.

Its main advantage is in terms of computation time, which grows linearly with the number of arguments evaluated (in most cases).

Characteristics:

The PLC-type state machine driver provides a solution to the problem of designing re-configurable and reusable state machines. However, this approach has also some shortcomings:

It is necessary to carry out the logical design of the state machine before implementing it in software. This might be a difficult task when implementing complex state machines having a great number of states and transitions.



Characteristics:

The PLC-type state machine driver provides a solution to the problem of designing re-configurable and reusable state machines.

Drawbacks:

- It is necessary to carry out the logical design of the state machine before implementing it in software.
- PLSs are not optimal in terms of execution time. They do not exploit the *locality of behaviour*.





State Logic Controller

Problems of non-optimality of PLCs can be eliminated with the other type of software architecture:

the State Logic Controller (SLC).

SLC are used to implement reconfigurable and reusable state machines.

State Logic Controller

The SLC is built around a data structure, which contains the machine-level representation of the formal model specifying system behaviour - a state transition graph.

SLC interprets the model, resulting in *direct* emulation of system behaviour. (vs. indirect emulation of PLCs).

System model is implemented as a table consisting of modified binary decision diagrams that represent the next-state mappings of various states, as specified by the state transition graph.

State Logic Controller

The SLC-type state machine driver is:

- → powerful
- it can be used to implement all types of :
 - sequential controller including synchronous (time-driven)
 - asynchronous (event-driven) state machines
- it can be extended to continuous and hybrid control systems as well as other applications.

Continuous Control Systems

Formal specifications of control systems (computational models)

Data-flow models

An *instruction / module* is executed when the operands required become available.

Control-flow models

An *instruction / module* executed when the previous *instruction / module* in a defined sequence has been executed.





Continuous Control Systems

Formal specifications of control systems (computational models)

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Continuous Control Systems

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History

Proposed by **Kahn** in 1958 as a formal model.

Data flow technique was originally developed in 1960s by **Karp** and **Miller** as graphicmeans of representing computations.

Unique attribute: deterministic

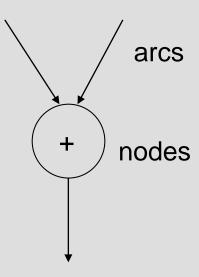
Applications of dataflow

- ♦ Block-diagram specifications
- Circuit diagrams
- Linear / Nonlinear Control Systems
- Signal processing
- Suggest dataflow semantics
- Common in Electrical Engineering

Data Flow Models

It uses a directed graph called:

a data dependence graph
or
a dataflow graph



Types:

- Objection is the result in phely incentae nice to a code filin in the interest in the int
 - > Alondoetse ffinee svhuetre na la lhipruptuttotkoetresn sa pypietra thæn slatime tare vioursberutappup etaken have been consumed.
 - Mipute to keens need not be consumed before pare vije unservije un
 - These rules allows pipeline computations and loops

 butandwegolopiopengedecheding not fixed though
 such as actions as recursion and code sharing there is a handshaking acknowledgement mechanism.
 - There is no requirement of acknowlegment mechanism.

Macrodataflow:

2. Refestion:

- **State of the analysis** of the second Mode freswire franting the operands are recieved
- The nodes represent procedures/functions, the hon-standard firing rule input tokens carry procedure/function parameters blader fer esupplier to kertain appenition expension residued. Each nodal operation is completed when all necessary operand are received.

Intuitive Semantics

- ♦ Determinater stateless) perform computation
- unique output sequences given unique input sequences
 Unbounded FIFOs perform communication via matrix of integer, float, fixed point sequences of tokens carrying values

 - integer, float, fixed point Blocking read -> process cannot test input queues
 - matrix of integer, float, fixagtpaist
 - image of pixels
- State implemented as self-loop

Kahn Process

The process is constrained to be continuous.

- \diamond Prefix ordering of sequences: $X \subseteq Y$
- ♦ Set of sequence can be ordered as well:

$$X \subseteq Y$$
, if $X_i \subseteq Y_i$ for $\forall i$

Increasing chain of sequences

$$\chi = \{ X_0, X_1, \ldots \},$$

where: $X_0 \subseteq X_1 \subseteq \dots$

Kahn Process

The process is constrained to be continuous.

- \diamond Least upper bound of $\chi : \cup \chi$
- \diamond Functional process *F*: $S^p \rightarrow S^q$:
 - Continuity

$$F(\cup \chi) = \cup F(\chi)$$

Monotonicity

$$X \subseteq X' \Rightarrow F(X) \subseteq F(X')$$

Reading an empty channel **blocks** until data is available.

Network of Processes

♦ A network: a set of relations between sequences.

$$X = F(X, I)$$

- Any X that forms a solution is called a fixed point. Continuity of F implies that there will be exactly one "minimal" fixed point.

Synchronous Dataflow (SDF)

Edward Lee and David Messerchmitt, Berkeley, 1987

Restriction of Kahn Networks to allow compile-time scheduling.

Basic idea:

Each process reads and writes a fixed number of tokens each time it fires.

Data Flow Systems

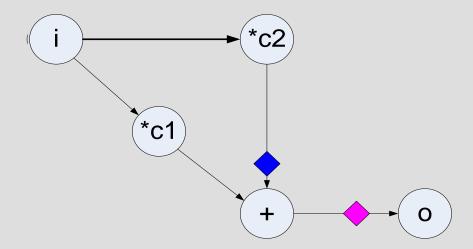
Synchronous Dataflow (SDF)

- ♦ Firing rules: Fixed token consumption/production
- Can be scheduled statically
 - Solve balance equations to establish rates
 - A correct simulation produces a schedule if one exists
- Looped schedules
 - For code generation: implies loops in generated code
 - Recursive SCC Decomposition

Data Flow Systems

Synchronous Dataflow (SDF)

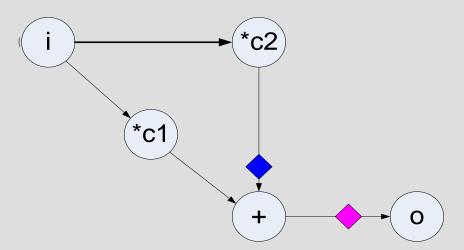
♦ Example:



Data Flow Systems

Synchronous Dataflow (SDF)

♦ Example: step-by-step execution



- Representing system reactions instead of data flow.
- An instruction / module executed when the previous instruction / module in a defined sequence has been executed.
- Data presence/absence has no influence to activation process

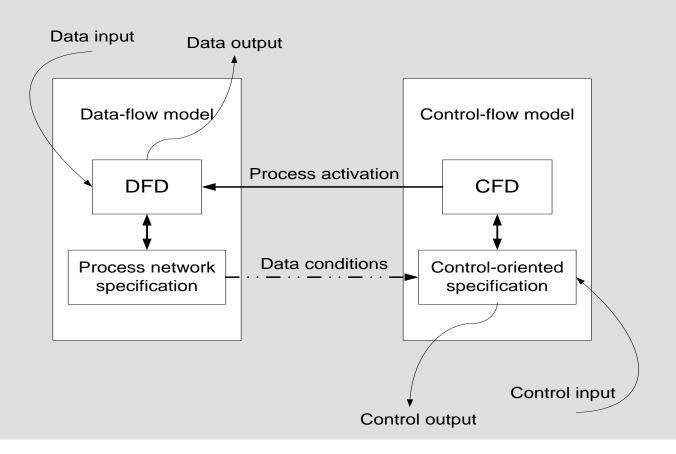
This model is very effective to represent event-driven systems.

The simplest model is FSM.

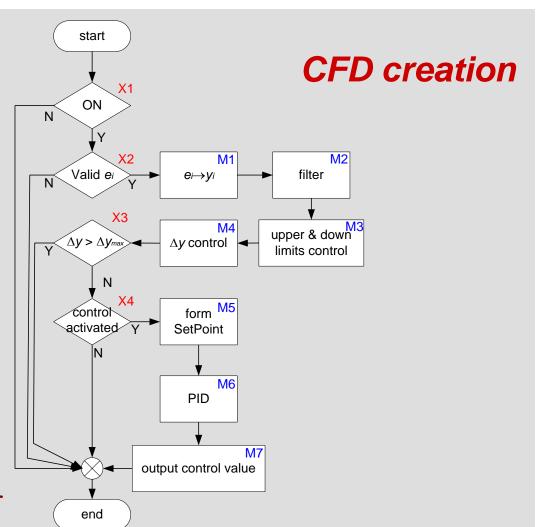
Steps in building CFM

- Remove data flows from data-flow diagram (DFD)
- Add control flows, stores, events and windows
- ♦ Events may be:
 - > sensor inputs
 - data conditions
 - switches and interrupts
 - signals from other programs

Relations between DFM and CFM



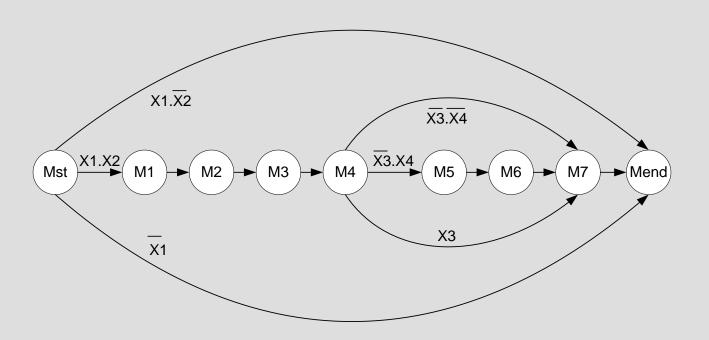




Flow-chart of PID contour

Example:

CFD creation

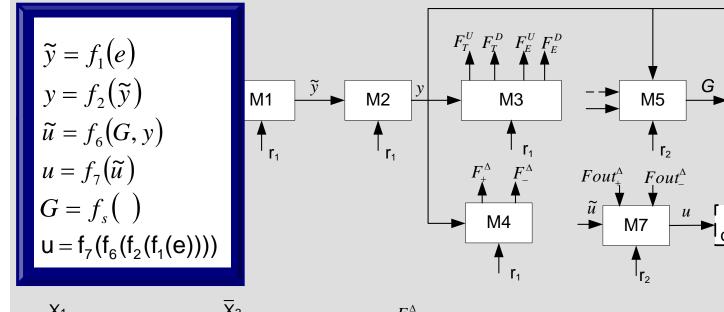


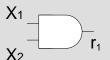
Control-flow graph



Example:

CFD creation





$$\overline{X}_3$$
 X_4

$$F_{-}^{\Delta}$$
 X3

Data-flow graph

M6

analog

output driver

Example:

CFD creation

Steps of work:

- 6. Missagregnemptæsdrivvetrobævetpteinstgmalltot od plessible
- 2. It conversion is correct with transforms be implemented at
- 7. Mattue PJD regulator it generates output signal \widetilde{u}
- 8. MZ ebintino desegnesi igrate blooks tep $(\widetilde{yt}, \forall a)$ \widetilde{u} to correspond to
- 4. While to be between technological and
- 9. Armælggenatplirhidsiver converts control value u to analog
- 5. Ma controls signal value to has gradient between upper and down limits



Hybrid control systems are reactive control systems that involve both continuous and discrete dynamics and continuous and discrete controls.

Possible approaches

- Two tier control system supervisory discrete automaton and number of sequential controllers
- Extended FSM possible to implement signal transformations (continuous control) as state activities.

The simplest solution

Designed by considering the continuous and discrete event systems separately - by suppressing either

Difficulties:

The interaction between the continuous and discrete event systems complicate analysis.

becomes a differential equation

Modelling by combining state machine(s) and sequential flow controllers

- Sydiffer Edition to the process of t
- * The control of Air and Discrete Control device (automaton) and number of Eprical Air and Formation of Controlled plant a different
- → Fequencial Bede of controlled plant a different controller is activated.
- System supervisor reacts to external events.
 It activates corresponding to the second of the second o

<u>Modelling by hybrid controllers – extended</u> <u>state machines</u>

Modern approach in system design.

Control system behavior is represented as extended form of Moore machine able to make signal transformations as node operations.

<u>Modelling by hybrid controllers – extended</u> <u>state machines</u>

1. Formal basis:

$$P = \{A, X, C, Y, E, R, S\},$$

A set of predicates, $C = \{ c_k \}$

A set of signal transformations, specifying the computation of output signals during the execution of the coresponding reactions

<u>Modelling by hybrid controllers – extended</u> <u>state machines</u>

2. Specification of system reactions

$$R = \{ r_i \}$$
,

where:

$$r_i: A \times E \times C \rightarrow Y$$

Modelling by hybrid controllers – extended state machines

3. Specification of signal transformations

Signal transformation functions specify how the output signals are generated within the corresponding system reactions

$$\forall y_k \in Y \leftrightarrow s_k \in S$$

 $s_k : X_k(t) \quad y_k(t), X_k \subseteq X$

 s_k may be represented as a composition of simple functions,

i.e.:
$$y_k = w_l^k \quad w_{l-1}^k \quad w_{l-2}^k$$
...... w_1^k

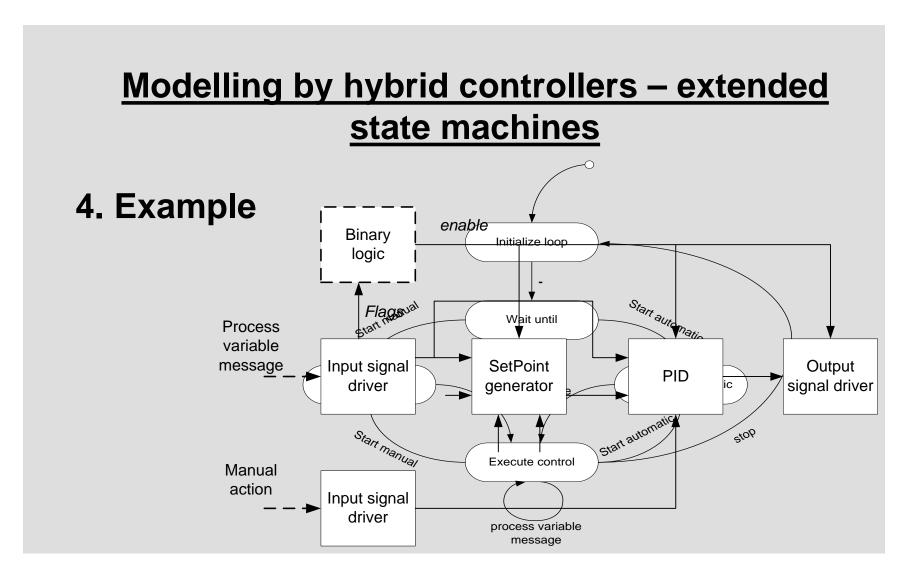


<u>Modelling by hybrid controllers – extended</u> <u>state machines</u>

3. Specification of signal transformations

Combination of system reactions defined as for Moore machine and signal transformations as dataflow leads to new hybrid (extended) Moore machine.







Graphic Notations and Languages

- Specification languages
 - ♦ UML
 - ♦ SDL
 - ♦ VHDL
- Languages defined in standards IEC 61131 and IEC 61499

- The Unified Modelling Language (UML), is the language that can be used to model systems.
- Unified Modeling Language is:
 - An emerging standard for modeling object-oriented software.
 - Resulted from the convergence of notations from three leading object-oriented methods:
 - OMT (James Rumbaugh)
 - OOSE (Ivar Jacobson)
 - Booch (Grady Booch)



- UML provides the ability to capture the characteristics of a system by using notations.
- UML provides a wide array of simple, easy to understand notations for documenting systems based on the object-oriented design principles.
- UML does not have any dependencies with respect to any technologies or languages.
- UML can be used to model applications and systems based on either of the current hot technologies.

Diagrams

The underlying premise of UML is that no one diagram diagram saniagpawie the different elements of a system in its entirety. Hence, UML isomator at Pon of hine birding that can be used that a system at different points of time in the software life cycle of a system. diagram

Activity diagram

Deployment diagram

Diagram Classification:

A software system can be said to have two distinct characteristics:

- → a structural ("static") part
- ♦ a behavioural ("dynamic") part.

An additional characteristic of a software system possesses is related to implementation.



Diagram Classification:

- Static this is essentially the structural aspect of the system. It defines what parts the system is made up of.
- Dynamic this is behavioural features of a system
- Implementation describes the different elements required for deploying a system

Diagram Classification:

- ♦ **Bhyptiærnie**ntation
 - Deje ptartiegthing ram
 - > Emsessinggrafiagram
 - The state of a system is the system is a system behaves in response to certain events or actions are the dynamic characteristics of a system.



Production life-time view:

- ♦ Design View
- ♦ Process View
- Component View
- Deployment View
- ♦ Use case View

Specification and Description Language (SDL) is a textual and graphical language that is both formal and object-oriented.

SDL is "an object-oriented, formal language ..." intended for the specification of:

- complex applications
- event-driven applications
- real-time applications
- interactive applications

involving many concurrent activities that communicate using discrete signals.

Main characteristics:

- Pirrovei dates tratecti roan ela sayannat pigue e olutso say estrente y stem.
- descriptionException handling (SDL 2000).
- Simulation, Validation, and Verification tools SDL is constructed in a manner to enable available for SDLs. description of system's behaviour in abstract terms.
- Conversion tools available to take SDL in and Theoretical model implemented is extended generate "useable code" independent FSMs running in parallel and
- Objetotuoi centitati day sightatsue echypnese concept
 (abstract data types).

Semantic models for system representation

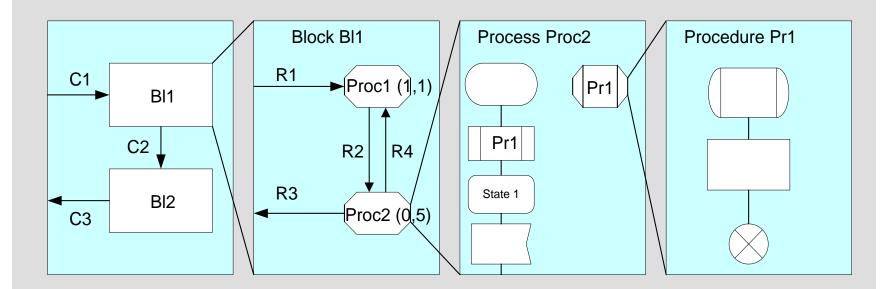
- Detaiteiouctefæseystesystem
 - Electronipolaticipataini en pira clesa testr, o commenculo atting for posterio atting the clesa testr, o commenculo atting for control atting the clesa testr, o commenculo atting the clesa testr.
 - ➤ Extended Finiten Station Violetwing the dep-down method of design

Program elements

- ♦ System block
- ♦ One or more Blocks
- Process (at least one)
- ♦ Procedure
- Processes can be dynamically allocated, blocks can not.



Relation among program elements



VHDL

VHDL means

Very High Speed Integrated Circuits Hardware Description Language

Basic definition

in Language Reference Manual (IEEE Design Automation Standards Committee, 1993a):

"...a formal notation intended for use in all phases of the creation of electronic systems. ...it supports the development, verification, synthesis and testing of hardware designs,...".



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in Language Reference Manual (IEEE Design Automation Standards Committee, 1993a)



VHDL is combination of programming language and hardware modelling language. When it was designed the main goal of VHDL was to simulate circuits.

Now it is used not only for simulation but for synthesis. Accounting current situation of VHDL implementations its abbreviation can be changed to VHSIC Hardware Design Language.

Language characteristics and elements

- Sequential Procedural language: inspired by ADA
- Concurrency: statically allocated network of processes
- Timing constructs
- Discrete-event simulation semantics
- Object-oriented elements: libraries, packages, polymorphism



One of most important parts of basic and extended versions of VHDL is time flow control.

Original version of VHDL is synchronous

❖ The module reacts by running the code of its

This is called scheduling a *transaction* on that signal.



VHDL is used outside electronics design. An extension VHDL-ACS supports simulation and description of circuits having continuous over time and over amplitude behaviour.

It is technologically independent.

VHDL is widely used for simulation / description / synthesis of FSMs.

For the needs of transitional systems analyses it simulates non-zero-time atomic operations, thus enabling time-correctness analyses.

VHDL is very useful for simulation and analyzes of parallel event-driven processes.



Main drawbacks

- it is hard for learning (except the user is not used in ADA)
- not all descriptions can be synthesized
- one and the same behaviour leads to different structures

The IEC 1131 standards were developed to be a common and open framework for PLC architecture, agreed to by many standards groups and manufacturers.

They were initially approved in 1992, and since then they have been reviewed as the IEC-61131 standards.



The main components

- ♦ IEC 61131-1 Overview
- ♦ IEC 61131-2 Requirements and Test Procedures
- ♦ IEC 61131-3 Data types and programming
- ♦ IEC 61131-4 User Guidelines
- ♦ IEC 61131-5 Communications
- ♦ IEC 61131-7 Fuzzy control

The programming models (IEC 61131-3) have the greatest impact on the user.

The IEC 1131-3 Standard

Common Elements

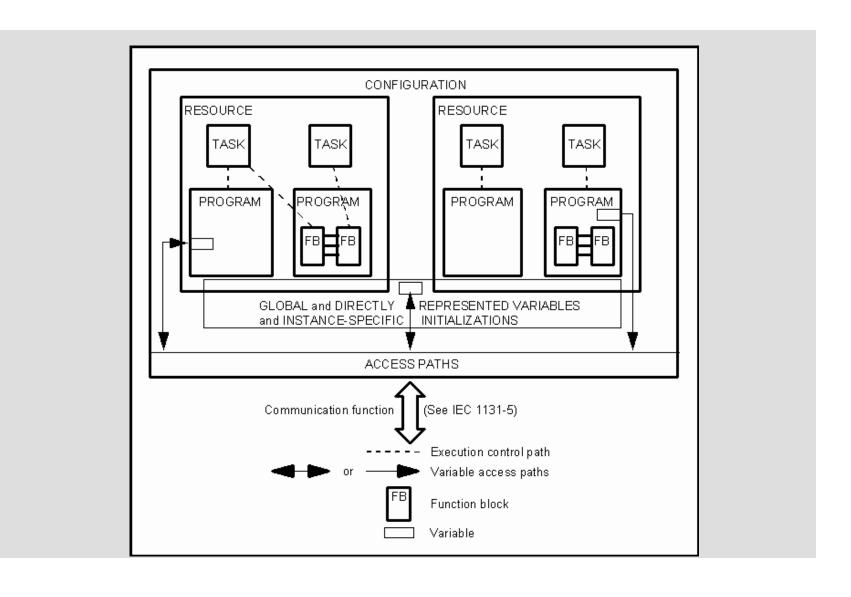
Programming Languages



Common Elements

- ♦ Data Type
- ♦ Variables
- Input variables
- Output variables
- ♦ Global variables
- Configuration, Resources and Tasks







Program Organization Units

- ♦ Functions
- → Function Blocks (FBs)
- ♦ Programs

Sequential Function Chart (SFC)

- SFC describes graphically the sequential behaviour of a control program.
- ♦ SFC structures

The internal organization of a program, and helps to decompose a control problem into manageable parts, while maintaining the overview.



Sequential Function Chart (SFC)

- ♦ SFC consists of :
 - > Steps

Each element can be programmed in any of the IEC languages, including SFC itself.

It is very similar to GRAFSET language.

A transition is associated with a condition, which, when true, causes the step before the transition to be deactivated, and the next step to be activated.





Programming Languages

- ♦ Textual:
 - Instruction List (IL)
 - Structured Text (ST)
- ♦ Graphical:
 - Ladder Diagram (LD)
 - Function Block Diagram (FBD)
 - Sequential Function Chart (SFC)



Programming Languages

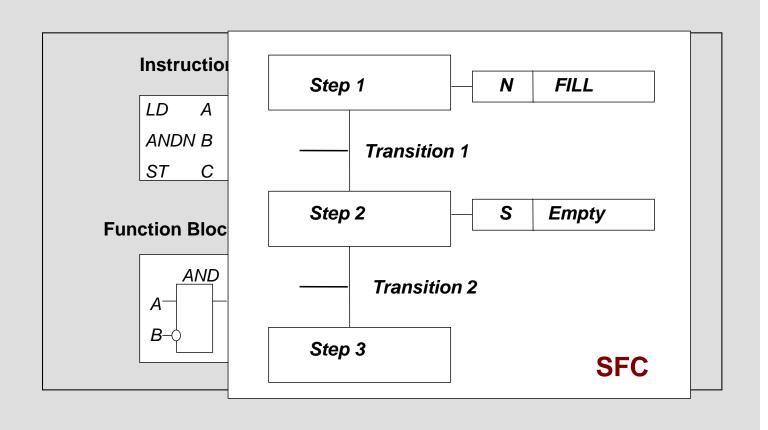
The choice of programming language is dependent on:

- the programmers' background
- what kind of the control problem
- the structure of the control system

All five languages are inter-linked: they provide a common suite, with a link to existing experience. In this way they also provide a communication tool, combining people of different backgrounds.



Programming Languages - examples





Top-down vs. bottom-up

Common Elements

Programming Languages

Top Down

Bottom Up

Advantages

- reduced waste of human resources, in training, debugging, maintenance and consultancy
- creating a focus to problem solving via a high level of software reusability
- reduced misunderstanding and errors
- programming techniques usable in a broad environment: general industrial control
- combining different components from different programs, projects, locations, companies



The standard IEC 61499 defines how function blocks can be used in distributed industrial process, measurement and control systems.

In industrial systems, function blocks are an established concept for defining robust, re-usable software components.



IEC 61499 defines a general model and methodology for describing functions blocks in a format that is independent of implementation.

The methodology can be used by system designers to construct distributed control systems.

It allows a system to be defined in terms of logically connected function blocks that run on different processing resources.





Phases in the design of a DCCS

Functional design phase

Process engineers analyze the physical plant design, to create the top-level functional requirements

Functional distribution phase

A further design phase is required to define the distribution of control functionality on to processing resources.





IEC 61499 is a multi-part standard be in development for a number of years.

- Part 1 covers the architecture and concepts for designing and modelling function block oriented systems
- Part 2 addresses the definition of a formal information models that will enable CASE tools and utilities to manipulate and exchange system designs based on function blocks.





Task-level Modeling

The END